## **REMARKS**

Claims 1-24 are presented for examination. Claim 1 has been amended to incorporate the subject matter of original claim 2. Claim 2 has been amended to further define the claimed invention.

Claim 11 has been corrected to address the objection.

The title of the invention has been found to be non-descriptive. A new title has been required. In accordance with the Examiner's suggestion, the title has been changed to --CACHE MEMORY SYSTEM HAVING HARDWARE AND SOFTWARE CACHE CONTROLLERS--.

Claims 1-6, 9-10, and 17-20 have been rejected under 35 U.S.C. § 102(b) as being anticipated by the Fujiwara publication entitled "A Custom Processor for the Multiprocessor System ASCA." Dependent claims 7-8 and 11-12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Fujiwara publication in view of the Handy publication entitled "The Cache Memory Book." Dependent claims 13-16 and 21-24 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Fujiwara publication in view of the Hallnor publication entitled "A Fully Associative Software-Managed Cache Design."

To more clearly define the claimed invention, claim 1 has been amended to incorporate the subject matter of claim 2. The rejection with respect to the subject matter of the original claim 2 has been respectfully traversed for the following reasons.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied*, 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted

definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." *In re Schaumann*, 572 F.2d 312, 197 USPQ 5 (CCPA 1978).

Claim 1, as amended, recites a cache memory system including a small-capacity cache memory which enables high-speed access and is provided between a processor and a main memory. The system comprises:

- a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software; and
- a hardware cache controller which performs hardware control for controlling data transfer to the cache memory by using a predetermined hardware.

The processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control.

The claim specifies that when a cache miss happens at the time of the software control, the processor causes the hardware cache controller to perform the hardware control.

The Examiner relies upon Section 3.1.3, lines 32-36 of the Fujiwara publication for disclosing this feature.

Considering the reference, the Fujiwara publication discloses that a custom microprocessor MAPLE changes a software cache control mode to a hardware cache control mode "if the data movements run off the predicted behavior."

Hence, the reference does not disclose that when a cache miss happens at the time of the software control, the processor causes the hardware cache controller to perform the hardware control.

Accordingly, the reference does not expressly disclose the claimed feature.

In the event the Examiner relied upon inherency without expressly indicating such reliance, the Examiner should be aware that inherency requires certainty, not speculation. *In re Rijckaert*, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); *In re Oelrich*, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); *In re Wilding*, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is **necessarily** present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. *In re Robertson*, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). The Examiner provided no factual basis upon which to conclude that a cache miss required by the claim <u>necessarily</u> happens when "the data movements run off the predicted behavior."

Moreover, one skilled in the art would understand that a cache miss does not necessarily occur when "the data movements run off the predicted behavior."

Accordingly, the reference neither expressly nor under the principles of inherency discloses that when a cache miss happens at the time of the software control, the processor causes the hardware cache controller to perform the hardware control.

Claims 2-24 dependent from claim 1 are defined over the reference at least for the reasons presented above in connection with claim 1.

Moreover, claim 2 has been amended to specify that when a cache miss happens at the time of the software control, the processor <u>automatically</u> causes the hardware cache controller to perform the hardware control.

10/0,76,625

This feature is not disclosed in the prior art of record. As disclosed in Section 3.1.3, lines

36-41 of the Fujiwara publication, "the mode alteration triggers a write back operation for

maintain (sic) consistence between data in cache and memory. After that, the hardware

controlled cache causes cold miss hit like starting up." Further, the reference explains that to

provide a remedy for this drawback, "the mode can be changed explicitly by the software with

executing a mode change instruction."

By contrast, the claimed invention enables the processor to automatically change the

cache's mode of operation when a cache miss happens at the time of the software control. As a

result, the claimed invention reduces the overhead of the cache's mode change.

In view of the foregoing, and in summary, claims 1-24 are considered to be in condition for

allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is

hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to

such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Alexander V. Yampolsky

Registration No. 36,324

600 13th Street, N.W.

Washington, DC 20005-3096

(202) 756-8000 AVY:MWE

Facsimile: (202) 756-8087

Date: February 12, 2004

12